

**WEST**

Your wildcard search against 2000 terms has yielded the results below

Search for additional matches among the next 2000 terms

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Search Results - Record(s) 1 through 10 of 35 returned.

☐ 1. Document ID: US 6269469 B1

L1: Entry 1 of 35

File: USPT

Jul 31, 2001

US-PAT-NO: 6269469

DOCUMENT-IDENTIFIER: US 6269469 B1

TITLE: Method and apparatus for parallel routing locking mechanism

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw Desc	Image
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☐ 2. Document ID: US 6263483 B1

L1: Entry 2 of 35

File: USPT

Jul 17, 2001

US-PAT-NO: 6263483

DOCUMENT-IDENTIFIER: US 6263483 B1

TITLE: Method of accessing the generic netlist created by synopsys design compiler

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw Desc	Image
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☐ 3. Document ID: US 6260183 B1

L1: Entry 3 of 35

File: USPT

Jul 10, 2001

US-PAT-NO: 6260183

DOCUMENT-IDENTIFIER: US 6260183 B1

TITLE: Method and apparatus for coarse global routing

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw Desc	Image
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☐ 4. Document ID: US 6260180 B1

L1: Entry 4 of 35

File: USPT

Jul 10, 2001

US-PAT-NO: 6260180  
DOCUMENT-IDENTIFIER: US 6260180 B1  
TITLE: System and method for detecting FETs that are susceptible to bootstrapping

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw Desc	Image
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☐ 5. Document ID: US 6253363 B1

L1: Entry 5 of 35

File: USPT

Jun 26, 2001

US-PAT-NO: 6253363  
DOCUMENT-IDENTIFIER: US 6253363 B1  
TITLE: Net routing using basis element decomposition

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw Desc	Image
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☐ 6. Document ID: US 6247167 B1

L1: Entry 6 of 35

File: USPT

Jun 12, 2001

US-PAT-NO: 6247167  
DOCUMENT-IDENTIFIER: US 6247167 B1  
TITLE: Method and apparatus for parallel Steiner tree routing

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw Desc	Image
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☐ 7. Document ID: US 6230306 B1

L1: Entry 7 of 35

File: USPT

May 8, 2001

US-PAT-NO: 6230306  
DOCUMENT-IDENTIFIER: US 6230306 B1  
TITLE: Method and apparatus for minimization of process defects while routing

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw Desc	Image
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☐ 8. Document ID: US 6209123 B1

L1: Entry 8 of 35

File: USPT

Mar 27, 2001

US-PAT-NO: 6209123  
DOCUMENT-IDENTIFIER: US 6209123 B1  
TITLE: Methods of placing transistors in a circuit layout and semiconductor device with automatically placed transistors

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw Desc	Image
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☐ 9. Document ID: US 6205572 B1

L1: Entry 9 of 35

File: USPT

Mar 20, 2001

US-PAT-NO: 6205572

DOCUMENT-IDENTIFIER: US 6205572 B1

TITLE: Buffering tree analysis in mapped design

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw Desc	Image
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☐ 10. Document ID: US 6175950 B1

L1: Entry 10 of 35

File: USPT

Jan 16, 2001

US-PAT-NO: 6175950

DOCUMENT-IDENTIFIER: US 6175950 B1

TITLE: Method and apparatus for hierarchical global routing descend

Full	Title	Citation	Front	Review	Classification	Date	Reference
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KWIC	Draw Desc	Image
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Terms	Documents
(( (rule same (check\$ or verif\$) )and (netlist and parameter )) and (gate and channel and(ratio or width or length) and transistor ) )	35

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10

Documents, starting with Document:

11

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